

REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 3 through 12, and 14 through 22, are now in this case. Claims 7, 21, and 22 are proposed to be amended. Claim 12 is proposed to be canceled.

Claims 3 through 6, 11, and 14 through 20 now stand allowed.

Claims 7 through 10 were objected to but were indicated as directed to patentable subject matter. Specifically claim 7 was objected to for reciting "valid" rather than "dirty", in its line 11, and claims 8 through 10 were objected to because they depend on claim 7. Claim 7 is amended to correct the deficiency noted by the Examiner. The amendment to claim 7 is supported by the specification,¹ and therefore no new matter is presented. Applicant respectfully submits that claims 7 through 10 are now in condition for allowance.

Claim 12 was finally rejected under §102 as anticipated by Goodman.² Claim 12 is proposed to be canceled, obviating the rejection.

Claims 21 and 22 were finally rejected under §112, ¶1, as failing to comply with the written description requirement. The Examiner asserted that the specification support offered by Applicant in the last Amendment did not clearly support the claims.

Claims 21 and 22 are proposed to be amended to independent form, incorporating the elements of previously presented claim 12, upon which they depended. Applicant respectfully submits that each of these claims 21 and 22 are fully supported by the specification, and accordingly traverse the final rejection of these claims under §112.

¹ See specification of 09/932,381, at page 31, paragraph [90].

² Goodman, *Memory Management for All of Us* (SAMS, 1992), pp. 119, 433-34.

Proposed amended claim 21 requires the step of starting a transferring of a block of data values, using the direct memory access controller, after the operating of the direct memory access controller to transfer the data value into the selected segment in the local memory that occurred in response to the access of this segment by the processor, but with the indicator bit for that segment not being valid.

The method of amended claim 21 corresponds to an alternative embodiment of the invention described in the specification.³ Specifically, the described exemplary implementation refers to the CPU accessing local memory, in which the valid bit for the accessed location is not set (e.g., step 922 detects a "miss"), following which "a block operation is commenced" through the operation of step 924 (and "arc 925").⁴ More specifically, claim 21 refers to the case in which "block initiation" is provided by step 924, with no block transfer initiation step (e.g., step 900) otherwise provided, as clearly stated by the last sentence of paragraph [0067] of the specification as filed.⁵

Applicant therefore respectfully submits that the method of proposed amended claim 21 is fully supported by the specification.

Proposed amended claim 22 is directed to an alternative method in which the block transferring of data using the direct memory access controller is separately initiated, such that the step of operating the processor to access a segment in the local memory is performed during the block transferring step. The claimed method further requires the operating of the direct memory access controller to transfer data to the selected segment, responsive to the state of the indicator bit for the addressed segment not being valid, followed by the restarting of the transferring step after the data value has been transferred to the selected segment.

³ Specification, *supra*, paragraphs [66] and [67], corresponding to U.S. Patent Application Publication No. US 2002/0078268 A1, paragraphs [0103] and [0104].

⁴ Specification, *supra*, paragraph [66], corresponding to published paragraph [0103].

⁵ Specification, *supra*, paragraph [67], corresponding to published paragraph [0104].

This claimed method is also clearly described in the specification.⁶ As described thereat, the block operation is initiated in step 900,⁷ and the CPU can continue to execute operations during this block operation, such as by way of step 920 to access a memory address within the block being transferred.⁸ If a "hit-miss" occurs as a result of this access, then data is transferred to the CPU-accessed segment,⁹ following which the block transfer is then restarted (in this example of the specification, from the "miss" address from step 922).¹⁰

Applicant therefore respectfully submits that proposed amended claim 22 is fully supported by the specification, and accordingly respectfully traverses the final rejection of this claim on this basis.

Applicant further respectfully submits that both of proposed amended claims 21 and 22 are patentably distinct over the Goodman reference, asserted against claim 12 upon which these claims previously depended, and over the other prior art of record in this case.

The references cited by the Examiner as pertinent but not applied have been considered, but are not felt to come within the scope of the claims in this case.

The Examiner is invited to call the undersigned if a telephone interview would be helpful to advance the prosecution of this case.

⁶ Specification, *supra*, paragraphs [60] through [66], corresponding to published paragraphs [0097] through [0103].

⁷ Specification, *supra*, paragraph [60], corresponding to published paragraph [0097].

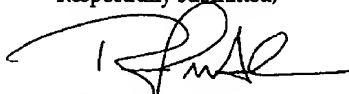
⁸ Specification, *supra*, paragraph [63], corresponding to published paragraph [0100].

⁹ Specification, *supra*, paragraph [65], corresponding to published paragraph [0102].

¹⁰ Specification, *supra*, paragraph [103], corresponding to published paragraph [0103].

For these reasons, Applicant submits that, upon entry of this amendment, all claims now in this case will be in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,



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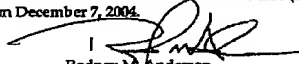
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